PATENT ABSTRACTS OF JAPAN

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(71)Applicant : KAWASAKI STEEL CORP

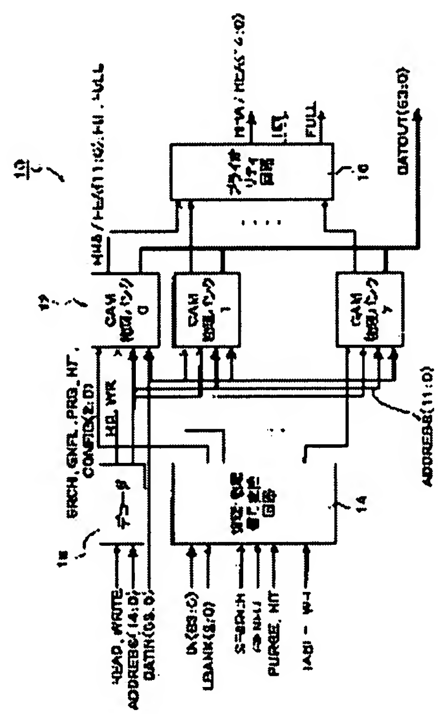
(72)Inventor : YOSHIZAWA HIROSHI
YONEDA MASATO

(54) ASSOCIATIVE MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an associative memory which has nothing useless in terms of cost and is easy to control in a system using plural associative memory of which the constitution is different.

SOLUTION: An associative memory array is divided into plural physical banks, each physical bank is constituted so as to be able to be set to different constitution, constitution of each physical bank is set, constitution of each logic bank is set corresponding to this setting, correspondence relation between each logic bank and each physical bank is allotted, each physical bank is controlled, retrieving is performed for each physical bank corresponding to each logic bank, and retrieved results outputted from each physical bank are outputted successively conforming to priority previously set by a priority circuit.



LEGAL STATUS

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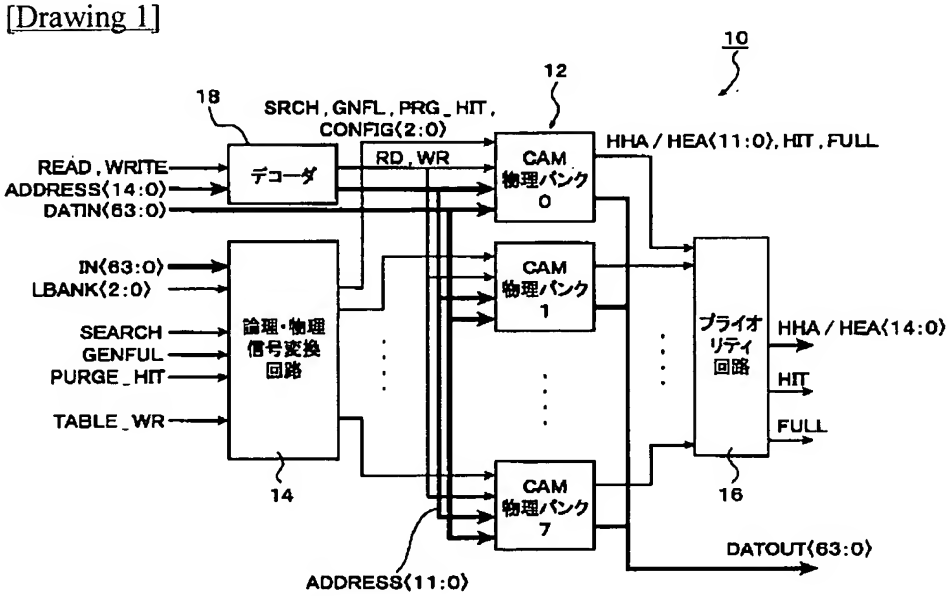
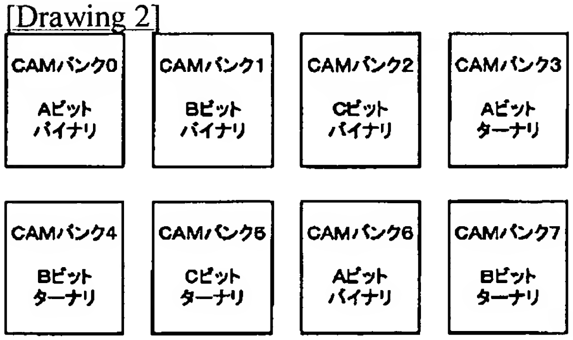
DRAWINGS

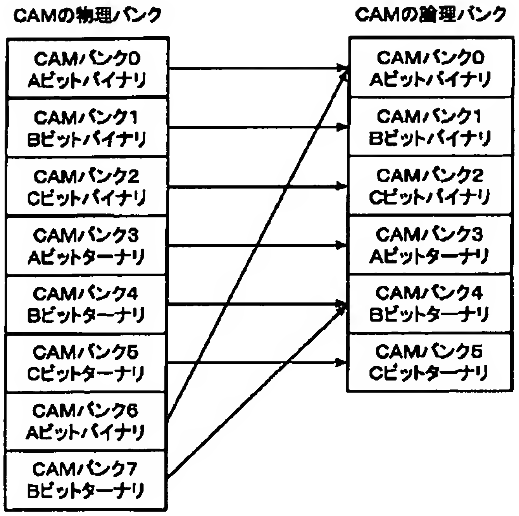
[Drawing 1]



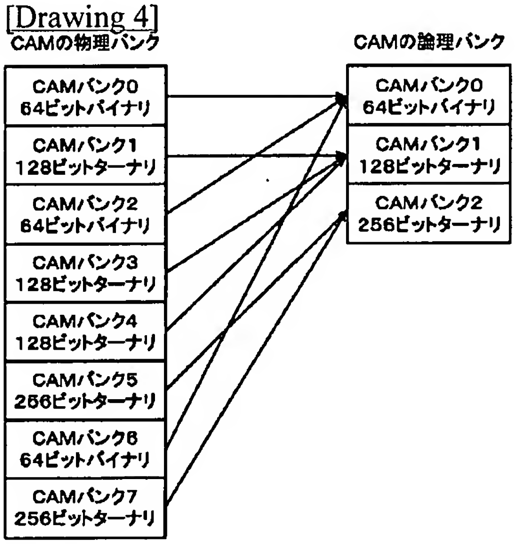
[Drawing 2]



[Drawing 3]



[Drawing 4]



[Drawing 9]

	CONFIG(2:0)
64ビットバイナリ	000
128ビットバイナリ	001
256ビットバイナリ	010
64ビットターナリ	100
128ビットターナリ	101
256ビットターナリ	110

[Drawing 5]

	物理バンク0	物理バンク1	物理バンク2	物理バンク3	物理バンク4	物理バンク5	物理バンク6	物理バンク7	テーブル構成
論理バンク0	Assign	No assign	Assign	No assign	No assign	No assign	Assign	No assign	64ビットバイナリ
論理バンク1	No assign	Assign	No assign	Assign	Assign	No assign	No assign	No assign	128ビットターナリ
論理バンク2	No assign	No assign	No assign	No assign	No assign	Assign	No assign	Assign	256ビットターナリ
論理バンク3	No assign	No assign	No assign	No assign	No assign	No assign	No assign	No assign	Not used
論理バンク4	No assign	No assign	No assign	No assign	No assign	No assign	No assign	No assign	Not used
論理バンク5	No assign	No assign	No assign	No assign	No assign	No assign	No assign	No assign	Not used
論理バンク6	No assign	No assign	No assign	No assign	No assign	No assign	No assign	No assign	Not used
論理バンク7	No assign	No assign	No assign	No assign	No assign	No assign	No assign	No assign	Not used

[Drawing 6]

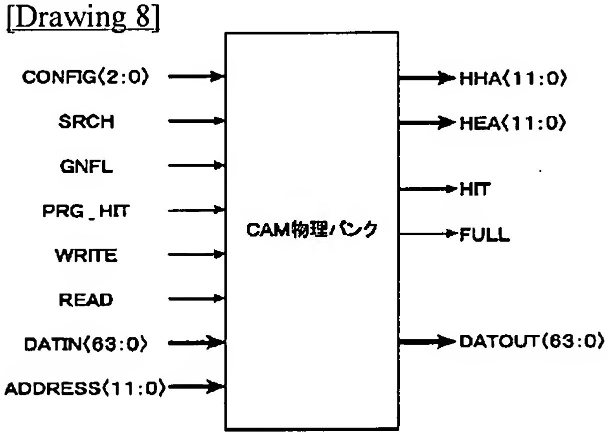
	物理バンク0	物理バンク1	物理バンク2	物理バンク3	物理バンク4	物理バンク5	物理バンク6	物理バンク7	テーブル出力
論理バンク0	1	0	1	0	0	0	1	0	10100010
論理バンク1	0	1	0	1	1	0	0	0	01011000
論理バンク2	0	0	0	0	0	1	0	1	00000101
論理バンク3	0	0	0	0	0	0	0	0	00000000
論理バンク4	0	0	0	0	0	0	0	0	00000000
論理バンク5	0	0	0	0	0	0	0	0	00000000
論理バンク6	0	0	0	0	0	0	0	0	00000000
論理バンク7	0	0	0	0	0	0	0	0	00000000

Assign="1"
No assign="0"

[Drawing 7]

	物理バンク0	物理バンク1	物理バンク2	物理バンク3	物理バンク4	物理バンク5	物理バンク6	物理バンク7
論理バンク0	ビット<0>	ビット<1>	ビット<2>	ビット<3>	ビット<4>	ビット<5>	ビット<6>	ビット<7>
論理バンク1	ビット<8>	ビット<9>	ビット<10>	ビット<11>	ビット<12>	ビット<13>	ビット<14>	ビット<15>
論理バンク2	ビット<16>	ビット<17>	ビット<18>	ビット<19>	ビット<20>	ビット<21>	ビット<22>	ビット<23>
論理バンク3	ビット<24>	ビット<25>	ビット<26>	ビット<27>	ビット<28>	ビット<29>	ビット<30>	ビット<31>
論理バンク4	ビット<32>	ビット<33>	ビット<34>	ビット<35>	ビット<36>	ビット<37>	ビット<38>	ビット<39>
論理バンク5	ビット<40>	ビット<41>	ビット<42>	ビット<43>	ビット<44>	ビット<45>	ビット<46>	ビット<47>
論理バンク6	ビット<48>	ビット<49>	ビット<50>	ビット<51>	ビット<52>	ビット<53>	ビット<54>	ビット<55>
論理バンク7	ビット<56>	ビット<57>	ビット<58>	ビット<59>	ビット<60>	ビット<61>	ビット<62>	ビット<63>

[Drawing 8]



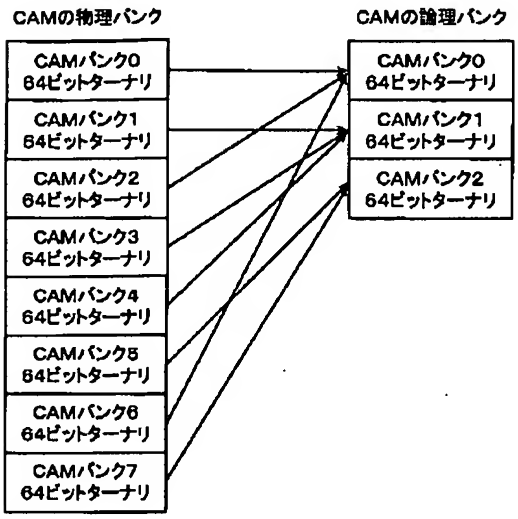
[Drawing 10]

物理バンク0 Hit	物理バンク1 Hit	物理バンク2 Hit	物理バンク3 Hit	物理バンク4 Hit	物理バンク5 Hit	物理バンク6 Hit	物理バンク7 Hit	HHA<11:0> 選択について
0	X	X	X	X	X	X	X	バンク0
1	0	X	X	X	X	X	X	バンク1
1	1	0	X	X	X	X	X	バンク2
1	1	1	0	X	X	X	X	バンク3
1	1	1	1	0	X	X	X	バンク4
1	1	1	1	1	0	X	X	バンク5
1	1	1	1	1	1	0	X	バンク6
1	1	1	1	1	1	1	0	バンク7

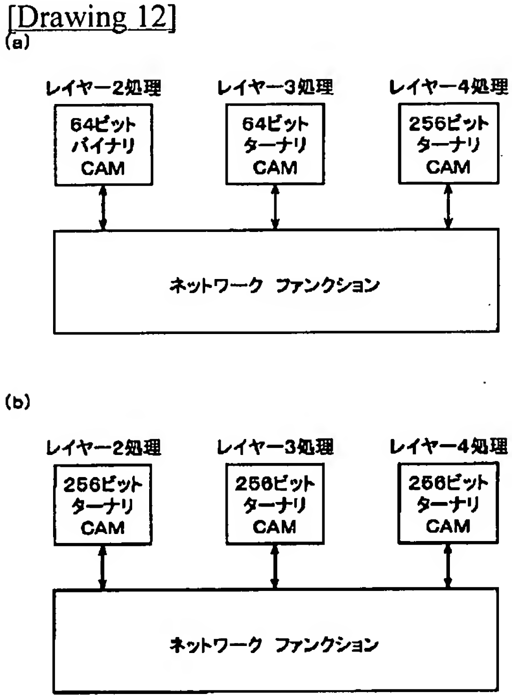
ヒット有り="0"
ヒット無し="1"

Don't care="X"

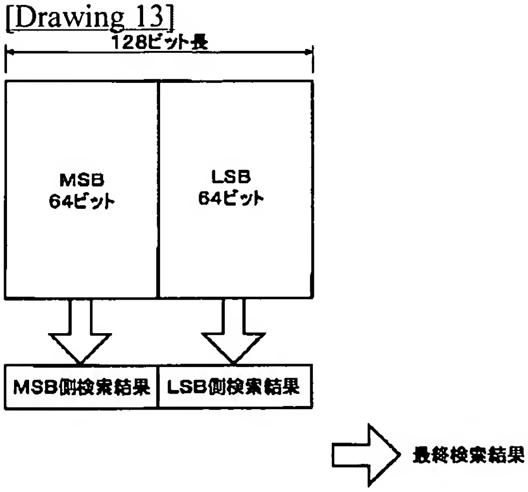
[Drawing 11]



[Drawing 12]



[Drawing 13]



[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the configuration schematic diagram of one example of the associative memory of this invention.
[Drawing 2] It is the conceptual diagram showing the condition of having set up the configuration of each the physical bank of each of one example.
[Drawing 3] It is the conceptual diagram showing the condition of having assigned the correspondence relation between each logic bank and each physical bank of one example.
[Drawing 4] It is the conceptual diagram showing the correspondence relation between each logic bank and each physical bank of one example.
[Drawing 5] It is the table of one example showing the correspondence relation between each logic bank and each physical bank.
[Drawing 6] It is the table showing the correspondence relation between each logic bank and each physical bank of one example.
[Drawing 7] It is the table of one example showing the relation between the table of drawing 8 , and each bit of Signal IN <63:0>.
[Drawing 8] It is the conceptual diagram showing the signal connected to a physical bank of one example.
[Drawing 9] It is the table of one example showing correspondence with Signal CONFIG <2:0> and the configuration of a physical bank of an associative memory array.
[Drawing 10] It is the table of one example showing the priority during a physical bank.
[Drawing 11] It is the conceptual diagram showing the correspondence relation between each logic bank and each physical bank of another example.
[Drawing 12] (a) And (b) is the configuration schematic diagram of an example using the conventional associative memory of a system.
[Drawing 13] It is the configuration schematic diagram of an example using the conventional associative memory of a system.
[Description of Notations]
10 Associative Memory
12 Associative Memory Array
14 Logic and Physical Signal Transformation Circuit
16 Priority Network
18 Decoder

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the associative memory which realizes the function of two or more associative memories of a configuration of differing with one device.
[0002]
[Description of the Prior Art] In recent years, rapidity and high efficiency are increasingly required by development of the Internet from the repeating installation which builds networks, such as a switching hub and a router. Since it corresponds to such a demand, with these equipments, the associative memory (CAM:Content Addressable Memory) has been used, for example for processing of classification processing (classification) of address filtering and a packet etc. more often.
[0003] CAM is used in many cases also with each layer of the layers 2, 3, and 4 of a network OSI (Open Systems Interconnection) model. In this case, the die length of search key data has thing various [to 32-256 bits or more] and sufficient with the configuration with conventional '0' and the data of '1' of Binary (Binary) CAM as a function of CAM, and what has the required function of the ternary (Ternary) CAM configuration which has data of 'X (Don't care)' in addition to this.
[0004] Therefore, as shown in drawing 12 (a), a required function is received with layers 2-4. it being alike, respectively, and in the case of the suitable device of a configuration of differing, and the example of illustration, Ternary (64-bit binary CAM and 64 bits) CAM and the 256-bit ternary CAM being used, or Or as shown in this drawing (b), the function of Ternary CAM was substituted for the function of binary CAM, and, in the case of the device of the same configuration of big size, and the example of illustration, it has realized using three 256-bit ternaries CAM.
[0005] In the example of above-mentioned drawing 12 (a), since CAM which was adapted for each function is used, a pipeline can do each processing, but when the block of the network function which controls ****** CAM consists of LSI of a fraction or one chip, the increment in the signal pin to CAM poses a problem. Moreover, in recent years, mass CAM was in use, and since small CAM of memory space was not manufactured, as shown in this drawing (b), it had the problem that mass CAM had to be carried vainly.
[0006] Moreover, in the example of this drawing (b), in order to satisfy all to CAM of many bits For example, when realizing the table of 64 bit length by CAM of 128 bit length, as shown in drawing 13 After carry out division registration of the data at the MSB (most significant bit) and LSB (least significant bit) side, carrying out the mask of the LSB side, searching the MSB side, carrying out the mask of the MSB side conversely and searching the LSB side, processing in the exterior of obtaining a result is needed. Therefore, there was a trouble that an external circuit became complicated.
[0007]
[Problem(s) to be Solved by the Invention] The purpose of this invention cancels the trouble based on said conventional technique, does not have futility in cost in the system which uses two or more associative memories from which a configuration differs, and is to offer the associative memory which is easy to control.

[0008]
[Means for Solving the Problem] The associative memory array constituted possible [a setup in a configuration which this invention is divided into two or more physical banks, and is different in said each bank of physics] in order to attain the above-mentioned purpose, The logic and the physical signal transformation circuit which sets up the configuration of said each bank of physics, sets up the configuration of each logic bank corresponding to this, assigns the correspondence relation between each [these] logic bank and each physical bank, and controls said each bank of physics, About the retrieval result which searches to said physical bank corresponding to said logic bank, and is outputted from said each bank of physics The associative memory characterized by having the priority network which carries out a sequential output according to the priority set up beforehand is offered.
[0009]
[Embodiment of the Invention] Below, based on the suitable example shown in an attached drawing, the associative memory of this invention is explained at a detail.
[0010] Drawing 1 is the configuration schematic diagram of one example of the associative memory of this invention. The associative memory (henceforth CAM) 10 of this invention is what was constituted so that one device could realize the function with the difference in the class of binary CAM / ternary CAM, and the difference in bit length of two or more CAM of a configuration of differing, and as shown in this drawing, it is equipped with the associative memory array 12, logic and a physical signal transformation circuit 14, the priority network 16, and the decoder 18.
[0011] First, the associative memory array 12 consisted of two or more physical banks by which block division was carried out, and, in the case of the example of illustration, is divided into eight blocks to the physical banks 0-7. The configuration of each physical bank can be set as the bit length of arbitration out of two or more kinds of bit length which can set up whether it is used as binary CAM or ternary CAM according to the signal CONFIG inputted from logic and the physical signal transformation circuit 14, and is prepared beforehand.
[0012] Then, logic and the physical signal transformation circuit 14 respond to the configuration of CAM to need. By setting up the configuration of each physical bank of the associative memory array 12, setting up the configuration of each logic bank corresponding to this, and assigning the correspondence relation between each [these] logic bank and each physical bank of the associative memory array 12 Each physical bank of the associative memory array 12 is controlled so that access is correctly performed to each physical bank of the associative memory array 12 corresponding to each logic bank.
[0013] Here, Signal IN <63:0>, Signal LBANK <2:0>, Signal SEARCH, Signal GENFUL, signal PURGE_HIT, and signal TABLE_WR are inputted into logic and the physical signal transformation circuit 14. Moreover, from logic and the physical signal transformation circuit 14, Signal SRCH, Signal GNFL, signal PRG_HIT, and Signal CONFIG <2:0> are outputted to each physical bank of the associative memory array 12.
[0014] Others [signal / which is inputted into the associative memory array 12 from logic and the physical signal transformation circuit 14 / each], The signal RD generated by Signal READ and Signal WRITE, Signal WR, The signal ADDRESS generated by the decoding circuit 18 from ADDRESS <14:12> which is the high order triplet of ADDRESS <14:0> <11:0> Signal DATIN <63:0> is inputted and Signal HHA <11:0>, Signal HEA <11:0>, Signal HIT, and Signal FULL are outputted from the associative memory array 12 to the priority network 16. Signal DATOUT <63:0> is doubled and outputted from the associative memory array 12.
[0015] Finally, according to the priority set up beforehand, a priority network 16 adds an address high order triplet to Signal HHA <11:0> and Signal HEA <11:0> which are inputted from the associative memory array 12, and carries out the sequential output of Signal HHA <14:0> and the signal HEA <14:0>. In this example, the priority of the physical bank 0 of the associative memory array 12 is the highest, priority becomes low one by one below, and the priority of the physical bank 7 considers as the lowest thing. Signal HIT and Signal FULL are doubled and outputted from the priority network 16.
[0016] In this invention, a physical bank is each block when dividing the associative memory array 12 into two or more blocks physically. On the other hand, a logic bank is what assigned the room of a

physical bank logically, two or more physical banks can be connected if needed, and this can also be used as one room. The room of a logic bank can be used by the concept of this logic bank, without being conscious of the room of each physical bank.
[0017] For example, as shown in drawing 2 , the physical bank 0 is set as binary CAM of A bit length. Like the following binary CAM of B bit length, and the physical bank 2 for the physical bank 1 Binary CAM of C bit length, The ternary CAM of B bit length and the physical bank 5 are set up for the ternary CAM of A bit length, and the physical bank 4, and binary CAM of A bit length and the physical bank 7 are set [the physical bank 3] up for the ternary CAM of C bit length, and the physical bank 6 as ternary CAM of B bit length.
[0018] And as shown in drawing 3 , binary CAM of A bit length which connected the physical banks 0 and 6 with the logic bank 0 is assigned, and the ternary CAM of binary CAM of binary CAM of the B bit length of the physical banks 1-3 and C bit length and A bit length is assigned like the following to the logic banks 1-3, respectively. Moreover, the ternary CAM of the B bit length who connected the physical banks 4 and 7 with the logic bank 4 is assigned, and the ternary CAM of C bit length of the physical bank 5 is assigned to the logic bank 5.
[0019] In CAM10 of this invention, according to the configuration of an associative memory to need, i.e., the class of CAM of whether to use as ternary CAM whether it is used as binary CAM, and required bit length, as shown in drawing 2 As it opts for the configuration of each physical bank of the associative memory array 12 and is shown in drawing 3 according to required numbers of words, the function of two or more CAM in which configurations differ is realizable with one device by connecting two or more physical banks and constituting each logic bank.
[0020] The example shown in drawing 4 - drawing 10 is given hereafter, and actuation of CAM10 of this invention is explained concretely.
[0021] First, drawing 4 is the conceptual diagram showing the correspondence relation of each logic bank and each physical bank in CAM10 of drawing 1 of one example. In the case of this example, as shown in this drawing, the physical banks 0, 2, and 6 are set up as binary CAM of 64 bit length, and the ternary CAM of 128 bit length and the physical banks 5 and 7 are set up for the physical banks 1, 3, and 4 as ternary CAM of 256 bit length like the following. In addition, about the detail of each physical bank, it mentions later.
[0022] Here, the configuration of each physical bank is set up by the signal CONFIG <2:0> outputted from logic and the physical signal transformation circuit 14 to each physical bank, as already stated. triplet x which this signal CONFIG <2:0> has in the interior of logic and the physical signal transformation circuit 14 -- it is defined by the register for eight pieces (illustration abbreviation), and each register is set up from the outside of CAM10 by giving signal TABLE_WR.
[0023] Moreover, in the example of illustration, the 256 bit length and the 2K-word ternary CAM which connect the physical banks 5 and 7 with the 128 bit length, the 6K-word ternary CAM, and the logic bank 2 which connect the physical banks 1, 3, and 4 with 64 bit length which connects the physical banks 0, 2, and 6 with the logic bank 0, and is obtained, 12K-word binary CAM, and the logic bank 1, and are obtained, and are obtained are assigned, respectively. The correspondence relation between each logic bank of drawing 4 and each physical bank is shown in the table of drawing 5 .
[0024] Assignment of a logic bank is performed by Signal LBANK <2:0>. The correspondence relation between a logic bank and a physical bank is defined by the logic physics translation table in the interior of logic and the physical signal transformation circuit 14 as shown in drawing 6 . This logic physics translation table corresponds to the correspondence-related table of each logic bank and each physical bank which are shown in drawing 5 , and '1' and '0' are set up respectively corresponding to 'Assign (assigning and being)' of drawing 5 , and 'No Assign' (with no assignment).
[0025] By giving signal TABLE_WR, the value inputted from Signal IN <63:0> is set to this logic physics translation table so that that correspondence relation may be expressed to drawing 7 . When a logic bank is specified by Signal LBANK <2:0> by setting up the contents for eight registers which define Signal CONFIG <2:0>, and the logic physics translation table of drawing 6 based on the correspondence relation between each logic bank and each physical bank, the physical bank

corresponding to this can be controlled.
[0026] Then, drawing 8 is the conceptual diagram showing the signal connected to a physical bank of one example. This drawing expresses the physical bank of the associative memory array 12 of CAM10 shown in drawing 1 , and each signal of CONFIG <2:0>, SRCH, GNFL, PRG_HIT, WRITE, READ, DATIN <63:0>, ADDRESS <11:0>, HHA <11:0>, HEA <11:0>, HIT, FULL, and DATOUT <63:0> is connected to a physical bank.
[0027] First, CONFIG <2:0> is a signal for setting up the configuration of a physical bank of the associative memory array 12. using it as using a physical bank as binary CAM, or ternary CAM in this example, as shown in the table of drawing 9 -- making the difference in the class of that CAM, and bit length into 64,128,256 bits -- according to that difference, the functional configuration of each physical bank can be specified out of six kinds with the signal of a triplet.
[0028] Next, ADDRESS <11:0> is an input signal which specifies the memory address of this physical bank. DATIN <63:0> is entry data and the search key entry-of-data signal over this physical bank. DATOUT <63:0> is the output signal which read the entry data stored in the physical bank.
[0029] WRITE is an input signal for writing the 64-bit signal inputted as DATIN <63:0> in the memory address specified by ADDRESS <11:0>. READ is an input signal for reading the entry data stored in the memory address of the physical bank specified by ADDRESS <11:0> as DATOUT <63:0>.
[0030] SRCH is an input signal which directs retrieval initiation to this physical bank. HIT is an output signal showing whether a hit entry, i.e., the entry data which are in agreement with search key data, exists in this physical bank as a result of coincidence retrieval. It becomes high-level only when in the case of this example it is set to a low level when at least one hit entry exists in entry data, and, as for HIT, one does not exist [a hit entry].
[0031] HHA <11:0> is the output signal of the hit address (Highest Hit Address) of the ranking of the highest priority. When the above-mentioned HIT serves as a low level and a hit entry exists as HHA <11:0> as a result of coincidence retrieval, the memory address in which the high hit entry of priority is stored most, i.e., the hit address of the ranking of the highest priority, is outputted. In the case of this example, the smallest address of the hit addresses is outputted.
[0032] PRG_HIT is an input signal for eliminating this hit entry, when HIT serves as a low level and a hit entry exists in this physical bank as a result of coincidence retrieval. GNFL is an input signal for searching the empty address (HEA:Highest Empty Address) of the ranking of the highest priority in this physical bank. HEA <11:0> is outputted by inputting this GNFL.
[0033] FULL is an output signal for meaning whether the memory address by which an empty entry, i.e., the effective entry data set as the object of coincidence retrieval, is not stored in this physical bank as a result of inputting the above-mentioned GNFL to this physical bank exists. In the case of this example, FULL serves as a low level, only when an empty entry does not exist at all, and when at least one empty entry exists, it becomes high-level.
[0034] Finally, HEA <11:0> is the output signal of the empty address of the above-mentioned ranking of the highest priority. As a result of inputting GNFL, when FULL becomes high-level and an empty entry exists in a physical bank as HEA <11:0>, it is the output signal of the memory address in which the empty entry with the highest priority is stored, i.e., the empty address of the ranking of the highest priority. The smallest address of the empty addresses is outputted in this example.
[0035] A physical bank of the example of illustration is the block of the associative memory array of a memory space 256K-bit ternary CAM configuration in 64 bit length and 4K words physically. For example, when this physical bank is set up as binary CAM of 128 bit length, two coincidence retrieval is performed using 64-bit different search key data, AND of a retrieval result is taken, and it is outputted as a final retrieval result. This operates as CAM of 128 bit length seemingly.
[0036] In this case, the numbers of words of a physical bank become 2K words of one half seemingly. Therefore, when 128 bit length and 4K-word CAM are required, two physical banks will be connected and it will be used as one logic bank. In addition, Ternary CAM can be used as binary CAM by setting up suitably the data of 'X (Don't Care)' of Ternary CAM. Moreover, in the case of CAM of 256 bit length, a total of four AND retrieval is performed.

[0037] In CAM10 shown in drawing 1 , Signal CONFIG <2:0>, Signal SRCH, Signal GNFL, signal PRG_HIT, Signal WR, Signal RD, Signal DATIN <63:0>, Signal ADDRESS <11:0>, Signal HHA <11:0>, Signal HEA <11:0>, Signal HIT, Signal FULL, and Signal DATOUT <63:0> are signals corresponding to each signal connected to the physical bank shown in drawing 8 .
[0038] in addition, the logic bank specified by Signal LBANK <2:0> when Signal SRCH, Signal GNFL, and signal PRG_HIT take the AND of the signal SEARCH inputted into logic and the physical signal transformation circuit 14, respectively, Signal GENFUL, signal PURGE_HIT, and the output from the logic physics translation table of drawing 6 -- it is -- in addition -- and it is the signal outputted to a logic physics translation table only to the physical bank where '1' is set up.
[0039] In CAM10 shown in drawing 1 , first, before performing coincidence retrieval, entry data are written in to each physical memory of the associative memory array 12 corresponding to each logic bank. To the memory address of the logic bank specified by Signal ADDRESS <14:0>, i.e., the memory address of the physical bank corresponding to this logic bank, when entry data give Signal WRITE, Signal DATIN <63:0> is written in.
[0040] When performing coincidence retrieval to the ternary CAM of the 128 bit length of the logic bank 1 as an example, the logic bank 1 is first specified as signal LBANK<2:0>= '001 (binary number)'. Setting [of assignment of a physical bank of the line corresponding to the logic bank 1 of the logic physics translation table of drawing 6] = '01011000' is outputted by this assignment, and Signal SRCH, Signal GNFL, and signal PRG_HIT are given only to the physical corresponding banks 1, 3, and 4.
[0041] For example, if search key data are inputted as DATIN <63:0>, and Signal SEARCH is inputted and initiation of retrieval is directed, from logic and the physical signal transformation circuit 14, Signal SRCH will be given only to the physical banks 1, 3, and 4, and coincidence retrieval will be started only on these physical banks 1, 3, and 4. Since the logic bank 1 was the ternary CAM of 128 bit length, as it was already described, two AND retrieval is performed using 64-bit different search key data.
[0042] Consequently, when the hit entry which is in agreement with the search key data of a total of 128 bit length exists in the entry data registered into these physical banks 1, 3, and 4, Signal HIT serves as a low level, from the physical corresponding banks 1, 3, and 4, the signal HHA <11:0> which is the hit address with which the hit entry is registered is outputted, and these Signals HIT and Signals HHA <11:0> are inputted into a priority network 16.
[0043] In addition, from the physical bank where a hit entry does not exist in the physical banks 1, 3, and 4, and the physical banks 0, 2, 5-7 where Signal SRCH is not given, high level is outputted as a signal HIT as a result of coincidence retrieval. In a priority network 16, the signal HIT inputted from each physical bank determines priority, and the signal HHA <14:0> which added the number triplet of the physical bank which had the ranking of the highest priority in the signal HHA of the ranking of the highest priority <11:0> to the high order is outputted. for example, the physical bank with the ranking of the highest priority -- '5' -- the triplet added will be set to '101' if it becomes. Moreover, it doubles and Signal HIT is also outputted.
[0044] In this example, priority is so high that the number of a physical bank is small as shown in the table of drawing 10 , for example, when a hit entry exists in the physical bank 1, irrespective of the condition of the physical banks 3 and 4, from a priority network 16, the signal HHA of the physical bank 1 <11:0> is outputted, and HHA <14:12> is set to '001'. Moreover, Signal HIT is what took the AND of the signal HIT inputted from each physical banks 0-7, and if a hit entry exists in either of the physical banks 0-7, it will serve as a low level.
[0045] If similarly the logic bank 1 is specified when searching the empty address, Signal GNFL will be given from logic and the physical signal transformation circuit 14 only to the physical banks 1, 3, and 4 corresponding to this. If Signal GENFUL is inputted and retrieval of the empty address is started, as mentioned above, Signal GNFL will be given only to the physical banks 1, 3, and 4, and retrieval of the empty address will be started in these physical banks 1, 3, and 4.
[0046] Consequently, the signal FULL of the physical banks 1, 3, and 4 where the empty address exists becomes high-level, and the signal HEA <11:0> which is the empty address is outputted from the physical corresponding banks 1, 3, and 4. In addition, from the physical bank where the empty address

does not exist in the physical banks 1, 3, and 4, and the physical banks 0, 2, 5-7 where Signal GNFL is not given, a low level is outputted as a signal FULL as a result of retrieval of the empty address.
[0047] In a priority network 16, the signal FULL inputted from each physical bank determines priority, and the signal HEA <14:0> which added the number triplet of the physical bank which had the ranking of the highest priority in the signal HEA of the ranking of the highest priority <11:0> according to the priority shown in the table of drawing 10 to the high order is outputted. Moreover, it doubles and Signal FULL is outputted. Signal FULL is what took the OR of the signal FULL inputted from each physical banks 0-7, and if the empty address exists in either of the physical banks 0-7, it will become high-level.
[0048] As mentioned above, since CAM10 of this invention divides the mass associative memory array 12 into the block of two or more physical banks and reconfigurates these physical banks as a logic bank, it can divide and use a large-scale associative memory according to a use application. Moreover, since the mass associative memory array 12 is divided and retrieval actuation is made to perform (i.e., since retrieval actuation is performed only to the physical bank corresponding to a logic bank), power consumption can be reduced.
[0049] In addition, what is necessary is not to limit this invention to this but just to have divided it into two or more physical banks, although the case where the associative memory array 12 is divided into eight physical banks is mentioned as the example in the example of illustration. Moreover, this is not limited, either, although bit length which can be set up was made into three 64,128,256-bit kinds in the example. Moreover, neither a setup of the configuration of a physical bank nor a setup of the correspondence relation between a logic bank and a physical bank is also limited at all, but another example can be freely set up, as shown in drawing 11 .
[0050] Moreover, the above-mentioned example mentions and explains two, the class of CAM whether it is binary CAM and whether it is Ternary CAM as an element which opts for the configuration of a physical bank, and bit length. However, this invention is good also as selectable as an element which is not limited to this, for example, opts for the configuration of the physical bank by functional differences other than this etc. Moreover, this invention should just contain at least one element as an element which opts for the configuration of a physical bank.
[0051] Furthermore, in this invention, although the associative memory array 12, logic and a physical signal transformation circuit 14, the priority network 16, and the concrete component circuit of a decoder 18 are not illustrated in the above-mentioned example, as long as these concrete circuitry is circuits which realize the function which it is not limited at all but is mentioned above, it may be the thing of what kind of configuration. Especially, although the case where it constituted using a register or a table was illustrated, logic and the physical signal transformation circuit 14 are not limited at all, but may be constituted using other circuits.
[0052] The associative memory of this invention is fundamentally above. As mentioned above, although the associative memory of this invention was explained to the detail, of course in the range which this invention is not limited to the above-mentioned example, and does not deviate from the main point of this invention, various amelioration and modification may be made.
[0053]
[Effect of the Invention] it constitutes possible [a setup] in a configuration which was explained to the detail above and which the associative memory of this invention divides a mass associative memory array into the block of two or more physical banks, and is [like] different in a physical bank of these each, and these physical banks are used, reconfigurating them as a logic bank. Thereby, it can be used according to a use application, being able to divide a large-scale associative memory, and since the function of two or more associative memories in which configurations differ is realizable with one device, cost is reducible according to the associative memory of this invention. Moreover, according to the associative memory of this invention, by the concept of a logic bank, since he does not need to be conscious of the room of a physical bank, there is an advantage that control is easy. Moreover, according to the associative memory of this invention, since retrieval actuation is performed only to the physical bank corresponding to a logic bank, the power consumption which always poses a problem can also be reduced by the associative memory in which all associative memory cells carry out simultaneous

operation.

[Translation done.]

* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The associative memory array constituted possible [a setup in a configuration which is divided into two or more physical banks, and is different in said each bank of physics], The logic and the physical signal transformation circuit which sets up the configuration of said each bank of physics, sets up the configuration of each logic bank corresponding to this, assigns the correspondence relation between each [these] logic bank and each physical bank, and controls said each bank of physics, The associative memory characterized by having the priority network which carries out a sequential output according to the priority set up beforehand about the retrieval result which searches to said physical bank corresponding to said logic bank, and is outputted from said each bank of physics.

[Translation done.]